A FEEDFORWARD LIMITED SWITCH DYNAMIC LOGIC CIRCUIT

ABSTRACT OF THE DISCLOSURE

The N channel field effect transistor (NFET) of the inverting output stage of a LSDL gate is split into a large NFET and a small NFET. The large NFET is coupled to a feedforward pulse so that it is turned ON only when the inverting output is a logic one. When the inverting output is a logic one, another inverting stage turns ON if the dynamic node evaluates to a logic zero. The dynamic node is inverted and coupled to the large NFET on the inverting output stage thus quickly pulling the inverting output to a logic zero. The small NFET is turned ON as a keeper device through the normal logic path. If the inverting data output is a logic zero the feedforward pulse is not generated. By making the largest NFET a pulsed device the other FETs are reduced in size resulting in leakage and switching power savings.